IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Nori FUKASAWA et al. Group Art Unit: 2827

Serial No.: 09/029,608 Examiner: David E. Graybill

Filed: May 15, 1998 Confirmation No.: 6285

For: METHOD AND MOLD FOR A MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND A METHOD FOR MOUNTING THE DEVICE

Attorney Docket No.: 980233
Customer Number: **38834**

DECLARATION UNDER 37 CFR 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Toshimi KAWAHARA, a citizen of Japan hereby declare and state:

I am one of the inventors of the above-identified application.

I am familiar with the prosecution of the application, including the outstanding Office Action dated March 18, 2004, and the prior art discussed therein.

I am the author of the paper "Super CSP^{tm}" published in IEEE Transactions on Advanced Packaging, vol. 23, No. 2, May 2000.

The data presented in that paper with regard to the physical and structural differences of a compression-molded resin layer as compared with the conventional non-compression-molded resin layer such as by a dispensing method is set forth herein.

The conventional molded packages need different mold dies according to package size, requiring manufacturers to make as many mold dies as package sizes. This makes conventional molding less flexible than liquid sealing for general use. However, a compression-molded resin layer overcomes this drawback. With a compression-molded resin layer, encapsulant covers the entire area of wafers, which come in standard sizes of 6, 8 and 12 inches. Thus, there is no need to prepare many different kinds of mold dies. The compression-resin mold forming encapsulation method is an excellent encapsulation method for several reasons. The compression-resin mold forming encapsulation method accommodates, for example, the flowing and hardening of materials at high temperatures and under the pressure as high as 100 atmospheres. This means that the mold forming encapsulation method permits the use of encapsulant with extremely high viscosity, including materials that are solid state at room temperatures.

Table I shows the example of reliability test results of packages (DIP, 42 I/O pins by 1.27 mm pitch) encapsulated by dispensing method using a liquid-type resin and by a transfer molding method (compression-resin molded). The liquid resins used for the evaluation were supplied by three companies (a, b, and c). As the Table I shows, the encapsulated die encapsulated by transfer molding method can be exceptionally strong and reliable. By comparison, the dispensing method uses materials that flow at room temperature and normal atmospheric pressure. This produces packaging that is not as strong. Furthermore, in the transfer molding method, hardening occurs under high pressure. The encapsulant is thus forced to make contact with the polyimide, making an excellent interface between the chip and encapsulant. In the early days of development of new encapsulation technology, we had investigated the possibility of using the conventional transfer molding technology. We did not find a suitable encapsulant for filling a cavity space greater than 200 mmØ with thickness of less than 100 μm on which more than 20,000 posts are arranged. The

thickness of encapsulant that is 100 μm or thinner required the use of an encapsulant with enhanced adherence. This meant leaving out mold release agent from the highly reliable encapsulant for transfer molds. The encapsulation method of the present invention, which basically consists of transfer molding and compression molding, appears to resolve these issues, enabling the formation of a layer of encapsulant that is both thin and reliable.

I and/or those under my supervision also evaluated the package and tested the mounting reliability. Evaluation of the package was performed using the ball grid array packages with 45 solder balls, 0.75 mm pitch. Tests are being devised for two kinds of land grid array packages. Table II shows the specification of packages used for the evaluation. The body size of the packages are both 4.5 mm x 9.00 mm. The single package unit passed the standard battery of temperature cycle tests, pressure cooker tests, high-temperature exposure tests and moisture sensitivity test as shown in Table III. Also, in terms of board level reliability, the package mounted on the board passed temperature cycle tests, the pressure cooker test, the bending test and free fall test, providing its reliability as shown in Table IV. No failures have occurred although the typical values of bump standoff are extremely low.

The formula of Coffin—Manson shows that thermal fatigue life- time of soldering interconnection is proportional to the square of bump standoff at least in the case of considering the plastic deformation region. When the chip with the same specification [45 I/O pins by 0.75 mm pitch, distance from neutral point (DNP) =3.23 mm] is directly mounted on the motherboard without underfilling resin, if the bump standoff height is not more over 400μm, the number of cycles at first failure does not exceed 1000, even if the mold T/C test condition of -40°C ↔ 125°C.

Table I

TABLE I
EXAMPLE OF RELIABILITY TEST (PTHB) RESULTS OF BGA PACKAGE ENCAPSULATED BY DISPENSING METHOD USING LIQUID-TYPE RESIN AND TRANSFER MOLDING METHOD

Sample : TEG
Evaluate Condition : 121°C/100%RH 2atm 6V 10MHz
Fail-threshold: Deteriorate of Transistor properties

	Dispensing			Transfer molding
	a	b	c	d
96 Hrs	4/27*	22/27*	22/27*	0/27
192Hrs	22/23*			0/27

* Decap & V.I : Al pad corrosion

Table II

TABLE II
SPECIFICATION OF PACKAGE USED FOR THE RELIABILITY TEST

Ball Diameter (mm)	Post Diameter (mm)	Substrate Pad Size (mm)	Solder Screen Aperture Size (mm)	Bump Standoff (μm)
Φ0.35	Φ0.35	Φ0.35	Φ0.35 × t0.15	212 (Typ.)
Φ0.45	Φ0.45	Φ0.45	Φ0.35 × t0.15	295 (Typ.)

Table III

TABLE III
RELIABILITY TEST RESULTS OF SINGLE PACKAGE UNIT

Test	Test Condition		Results
Temperature Cycle	-65/+150°C	N=10	500cyc. PASS
Pressure Cooker	+121°C/85%RH	N=10	168Hrs PASS
High Temp. Storage	+150°C/ in the air	N=10	500Hrs PASS
Moisture Sensitivity	JEDEC Level 3	N=10	PASS

* Pre-Condition: PB(+125°C/24Hrs) – +85°C/85%RH/24Hrs – IR Reflow(+240°C up)

Table IV

TABLE IV
RELIABILITY TEST RESULTS OF PACKAGE MOUNTED ON THE BOARD

Test	Test Condition		Results
Temperature Cycle	-55/+125°C	N=20	1000cyc. PASS
Pressure Cooker	+121°C/85%RH	N=10	168Hrs PASS
Bending	Bending Span 3mm Bending Speed 5mm/min	N=10	OVER 15mm
Cyclic Bending	Bending Span 3mm	N=4	OVER 10000cyc.
Free fall			OVER 50cyc. OVER 2000cyc.

The undersigned declares that all statements made herein of his/her own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signed this 10th day of August, 2004

Toshimi Kawahara

Toshimi KAWAHARA